REMARKS/ARGUMENTS

This is a Supplemental Amendment in response to an Office Action dated March 28, 2006 which in turn is in response to an Amendment filed 01/11/06 in response to an Office action dated 10/17/2005.

Status

Claims 1-20 are pending

Claims 1-19 are rejected

Claim 20 is withdrawn from consideration

The drawings are objected to.

Election

Claim 20 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 8-4-5.

Drawing Objection(s)

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the reference signs mentioned in the description at paragraphs 6 and 8-10. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

At paragraph [0006], the discussion is Lin 6,063,670. The reference numerals are Lin's, and are presented in parenthesis. This is an entirely normal procedure. The text is a quotation from Lin's Abstract.

The objected to numbers in paragraphs [0008] and [0009] are deleted.

The drawings need <u>not</u> be amended.

Rejection(s) under 35 USC 112, second paragraph

<u>Claims 3-6, 9 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More particularly,</u>

> In **claims 3** and **4** there is insufficient antecedent basis for the language "the first dielectric."
>
> ***amended herewith***
>
> The scope of **claim 5** is indeterminable because the claim is ungrammatical.
>
> ***amended herewith***
>
> In **claim 6**, the scope of the claim is unclear because the language, "consisting germanium" is ungrammatical.
>
> ***amended herewith***
>
> In **claim 9**, the scope of the language "oxide" is unclear because the language appears to be given a meaning repugnant to its usual meaning. Specifically, the claim recites, "the second gate oxide comprises . . . silicon nitride," but silicon nitride is not an oxide.

Please note that the terms gate oxide and dielectric are used interchangeably throughout the specification (consistent with industry standards).

[0032] First, the entire (both left- and right-hand portions) surface of the substrate 202 is pre-cleaned, such as with RCA. Then, a first gate oxide 204 (DIELECTRIC-1, compare 104) is formed (grown or deposited) on the entire surface of the substrate 102. The first gate oxide 204 is suitably silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) or high-k, and suitably has a thickness of approximately 5 - 25 Angstroms, such as 20 - 25 Angstroms. The first gate oxide 204 may be grown or deposited using known processes.

[0040] Next, a second dielectric (DIELECTRIC-2) 212 is grown. Gate oxide 204 is protected from damage during this step by the overlying layers of poly-Si 206 and hard mask 208. The second dielectric (gate oxide) 210 is suitably silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) or high-k material, grown by:

- rapid thermal oxidation (RTO) in NO, N2O, NH3, O2 (500-1100 degrees C); or
- plasma nitridation treatment on base oxide (25 - 800 degrees C);
- plasma oxidation; UV oxidation; atomic layer deposition.

Hence, although including nitride in the list of possible gate oxides may be opposed to its usual meaning, it is quite clear in the context of the patent application.

In **claim** 11, the language, "during the growing the step of growing" is incomprehensible.
amended herewith

Claims 3-5 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Also see In re Wilson, 424 F.2d 1382 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06.

The claims have been amended to overcome

Rejection(s) under 35 U.S.C. 102 and 103

Claims 1, 2, 6, 12 and 15-19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Jeong (6,780,715). More particularly,

At column 7, line 8 to column 8, line 14, Jeong discloses the following:

Method of forming different gate oxides on a semiconductor substrate, the substrate having a top surface, a first area and second area which is distinct from the first area, comprising: forming a first gate oxide 74 on the top surface of the substrate; depositing a first layer of polysilicon 75 over the first gate oxide; forming a hard mask 76 on top of the first layer of polysilicon; forming a soft mask 77 covering the first gate oxide, first layer of polysilicon and hard mask in the first area of the substrate; removing the hard mask, the first layer of polysilicon and the first gate oxide in the second area of the substrate, leaving the second area exposed; stripping the soft mask; inherently cleaning the exposed second area of the substrate "etched selectively by using the first photoresist pattern layer 77 as a mask, so that the substrate 70 in the memory region 72 and the boundary area of the logic region 71 is exposed"; growing a second gate oxide 78 on the top surface of the substrate in the second area; and removing the hard mask; depositing a second layer of polysilicon 79 over the second gate oxide; wherein: the hard mask comprises a material selected from the group consisting germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO_2, Si_3N_4, and other materials that are easy to remove from a silicon wafer without leaving a residue; wherein: the first gate oxide is thinner than the second gate oxide.

Method of forming gate oxides on a semiconductor substrate, the substrate having a top surface, a first area and second area which is distinct from the first area, comprising: forming a first gate oxide on the top surface of the substrate; protecting the first gate oxide from damage during subsequent processing steps by forming a sacrificial hard mask over a selected area of the first gate oxide; and then forming a second gate oxide; before forming

the sacrificial hard mask, depositing a first layer of polysilicon over the first gate oxide; then removing the sacrificial hard mask "The first capping layer 76, . . . are etched selectively by using the first photoresist pattern layer 77 as a mask, so that the substrate 70 in the memory region 72 arid the boundary area of the logic region 71 is exposed"; after removing the sacrificial hard mask, depositing a second layer of polysilicon over the second gate oxide; before forming the sacrificial hard mask, depositing a first layer of polysilicon over the first gate oxide; wherein: the second layer of polysilicon extends over the first layer of polysilicon.

<u>Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (6,780,715). More particularly,</u>

Jeong does not appear to explicitly disclose wherein: the hard mask has a thickness of approximately 300-500 Angstroms choosing an initial thickness for the hard mask to ensure that after stripping the soft mask, a thickness of greater than approximately 15 angstroms of hard mask material remains in place on the substrate.

Notwithstanding, as can be reasoned from well established legal precedent, it would have been an obvious mailer of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied prior art, the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima fade that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc.. 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1084), cert. denied, 169 U.S. 830, 225 USPQ 232 (1984); In re Dailey, :357 F.2d 669, 149 USPQ 47 (CCPA 1966).

To further clarify, the scope of the limitation, "choosing an initial thickness for the hard mask to ensure that after stripping the soft mask, a thickness of greater than approximately 15 angstroms of hard mask material remains in place on the substrate" is not limited to a step of stripping the soft mask, and, a thickness of greater than approximately 15 angstroms of hard mask material remains in place on the substrate, because the language, "to ensure that after stripping the soft mask, a thickness of greater than approximately 15 angstroms of hard mask material remains in place on the substrate" is a statement of intended purpose of the hard mask thickness that does not appear to result in a manipulative difference between the claimed mask and the mask of Jeong. Further, because the mask of Jeong appears to have the same structure as the claimed mask, it appears to be inherently capable of being used for the intended purpose, and the statement of intended purpose does not patentably distinguish the claimed mask from the mask of Jeong. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d :1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

<u>Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong as applied to claim 1, and further in combination with Radens (6,388,294). More particularly,</u>

Jeong does not appear to explicitly disclose wherein the second gate oxide comprises a

material selected from the group consisting of silicon dioxide (Si02), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material; wherein the second gate oxide has a composition that is different than a composition of the first gate oxide.

Nonetheless, at column 3, lines 25-33 and column 5, lines 24-49, Radens discloses wherein a gate oxide 106 comprises silicon dioxide (Si02); wherein a second gate oxide 170 has a composition that is different than a composition of the first gate oxide. Moreover, it would have been obvious to combine this disclosure of Radens with the disclosure of Jeong because it would provide the second gate oxide of Radens and permit optimization of thickness and formation conditions or different selected regions of the semiconductor substrate.

Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong as applied to claim 1, and further in combination with Radens (6,388,294). More particularly,

Jeong does not appear to explicitly disclose wherein the second gate oxide is grown by a process selected from the group consisting of: rapid thermal oxidation (RTO) in NO, N20, NH3, 02 (500-1100 degrees C); plasma nitridation treatment on base oxide (25 - 800 degrees C); plasma oxidation; UV oxidation; and atomic layer deposition; wherein the first gate oxide comprises a high-k material.

Nevertheless, at paragraph 6, Radens discloses wherein a gate oxide comprising a high-k material is grown by atomic layer deposition. Furthermore, it would have been obvious to combine this disclosure of Radens with the disclosure of Jeong because it would insure a uniform composition and thickness of the gate oxide.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong as applied to claim 1, and further in combination with Lin (6,063,760). More particularly,

Jeong does not appear to explicitly disclose wherein during growing the step of growing the

second gate oxide, a portion of the hard mask becomes oxidized; arid further comprising: removing the oxidized portion of the hard mask using an etch that will remove the oxidized portion of the hard mask without affecting the second gate oxide.

Notwithstanding, at 3, lines 4-24; and column 3, line 66 to column 4, line 19, Lin discloses during the step of growing a second gate oxide 30, a portion of the hard mask 22 becomes oxidized; and further comprising: removing the oxidized portion of the hard mask using an etch "water" that will remove the oxidized portion of the hard mask without affecting the second gate oxide. In addition, it would have been obvious to combine this disclosure with the disclosure of Jeong because it would it would prevent or minimize the first gate oxide from growing thicker.

Please note that USP 6,063,760 is not "Lin" and it has nothing to do with semiconductors. The correct number appears to be 6,063,670, referred to in the specification at [0006].

The Invention, Generally

The invention is generally directed to forming gate oxides having multiple thicknesses. Gate oxides having different thicknesses are formed on a semiconductor substrate by forming a first gate oxide on the top surface of the substrate, forming a sacrificial hard mask over a selected area of the first gate oxide; and then forming a second gate oxide. A first poly layer may be formed on the first gate oxide, under the hard mask. After the hard mask is removed, a second poly layer may be formed over the second gate oxide and over the first poly layer. This enables the use of high-k dielectric materials, and the first gate oxide can be thinner than the second gate oxide.

More particularly, as noted in the specification,

[0030] FIGs. 2A-2E illustrate an embodiment of a technique for forming multiple gate dielectrics on a semiconductor substrate 202 (compare 102). A sequence of steps and structures resulting therefrom are illustrated.

[0032] First, the entire (both left- and right-hand portions) surface of the substrate 202 is

pre-cleaned, such as with RCA. Then, a first gate oxide 204 (DIELECTRIC-1, compare 104) is formed (grown or deposited) on the entire surface of the substrate 102. The first gate oxide 204 is suitably silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) or high-k, and suitably has a thickness of approximately 5 - 25 Angstroms, such as 20 - 25 Angstroms. The first gate oxide 204 may be grown or deposited using known processes.

[0033] Then, a thin layer of polysilicon (also "poly-Si", or simply "poly") 206 which will function as a gate electrode is deposited on the entire exposed surface of first gate oxide 204, using known processes. The layer of polysilicon 206 suitably has a thickness of approximately 2-50 nm (20 - 500 Angstoms).

[0034] Then, a hard mask 208 is deposited on the entire exposed surface of the layer of polysilicon 206, using known processes. The hard mask 208 is suitably germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO2, Si3N4, or other materials that are easy to remove from a silicon wafer without leaving a residue. The hard mask 208 suitably has an initial thickness of approximately 30-50 nm (300-500 Angstroms). As will become evident, the hard mask is sacrificial in that after it serves the purpose of protecting the first gate oxide 204 from subsequent process steps, it can be removed, notably without damaging the subsequently formed second gate oxide (212, described hereinbelow).

[0035] Then, photoresist (PR) 210 (compare 106) is applied and patterned, forming a soft mask for further processing steps, so that a first portion (left-hand side, as viewed) of the stack of gate oxide 204 / poly-Si 206 / hard mask 208 is covered with photoresist 210 and a second portion (right-hand side, as viewed) is exposed - i.e., not covered with photoresist. The photoresist serves as a soft mask. The soft mask 210 covers the first gate dielectric, first layer of polysilicon and hard mask in the first area 202a of the substrate - i.e., a first gate oxide stack. The soft mask 210 leaves exposed the first gate dielectric, first layer of polysilicon and hard mask in the second area 202b of the substrate - i.e., a second gate oxide stack.

[0036] Then, the exposed areas of the hard mask 208 / poly-Si 206 and DIELECTRIC-1 206 are removed, using standard etching processes such as reactive ion etching (RIE) or wet etching, down to the surface of the substrate 202. The resulting structure is shown in the cross-sectional view of FIG. 2A.

[0037] Next, the photoresist 210 is stripped using standard techniques (e.g., mixture of H2SO4 and H2O2). During photoresist strip, the hard mask (Ge) 208' may be partially etched, for example having a thickness of approximately up to 50% less than shown in FIG. 2A. Therefore, the initial thickness of the hard mask 208 must be chosen to ensure that after photoresist strip, a sufficient thickness of hard mask remains. For example, a sufficient remaining thickness would be approximately at least 1.5 nm (15 Angstroms) left after PR strip. The thickness of the hard mask material that remains in place on the substrate after stripping the substrate should be sufficient to be consumed during the second oxidation process (described below) and not allow any poly-Si to be oxidized. Thus, the thickness depends on the second oxide thickness and process conditions.

[0038] The resulting structure is shown in the cross-sectional view of FIG. 2B wherein the slightly etched hard mask 208' is shown with a primed (') number indicating that it has been altered (in this case, thinned) between the views of FIGs. 2A and 2B.

[0039] Next, standard surface preparations are made for forming a second dielectric (DIELECTRIC 2). As is evident, the top of gate oxide 204 is protected from damage during this pre-clean step by the overlying layers of poly-Si 206 and hard mask 208.

[0040] Next, a second dielectric (DIELECTRIC-2) 212 is grown. Gate oxide 204 is protected from damage during this step by the overlying layers of poly-Si 206 and hard mask 208. The second dielectric (gate oxide) 210 is suitably silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) or high-k material, grown by:

- rapid thermal oxidation (RTO) in NO, N2O, NH3, O2 (500-1100 degrees C); or
- plasma nitridation treatment on base oxide (25 - 800 degrees C);

- plasma oxidation; UV oxidation; atomic layer deposition.

[0041] The second dielectric 212 has an exemplary thickness of approximately 35-40 Angstroms.

[0042] During this step, the hard mask (Ge) 208' on top of the DIELECTRIC-1 areas will be oxidized, and a layer of germanium oxide (GeO2) 214 will be formed. The resulting structure is shown in the cross-sectional view of FIG. 2C wherein the slightly oxidized hard mask 208" is shown with a double-primed (") number indicating that it has been altered (in this case, oxidized) between the views of FIGs. 2B and 2C.

[0043] It should be noted that the thin poly-Si 206 is also protected from oxidation from the overlying hard mask 208' (208"). It should also be noted that the thickness of the hard mask 208 should be chosen such that it is not entirely consumed by the oxidation process.

[0044] Next, the mask oxide (GeO2) 214 is removed using an etch that will remove the GeO2 without affecting (selective to) the second dielectric 212. For example, remove GeO2 with a water rinse since it is water soluble, which will not etch the second dielectric 212. Then, the remaining hard mask (Ge) material 208" is removed, selective to SiO2 and polysilicon. For example, remove the Ge with an H2O2 rinse. The resulting structure is shown in the cross-sectional view of FIG. 2D

[0045] Herein it should be noted that the thin polysilicon 206 has remained in place on top of the first gate oxide 204 throughout the process sequence. Since it is never removed, and remains part of the final structure, the thin polysilicon 206 serves to preserve the high quality of the first gate oxide 204. This enables, among other things, the use of high-k material for the first gate oxide 204.

[0046] Next, gate polysilicon 216 (for a second gate electrode) is deposited on top of the entire wafer 202, including the first gate oxide 204 which is already covered by a thin protective layer of polysilicon 206, and including on top of the second dielectric 212.

The gate polysilicon 216 may be deposited by a standard process such as low pressure chemical vapor deposition (LPCVD; furnace) or room temperature chemical vapor deposition (RTCVD; single wafer reactor) with SiH4 or other silicon precursor. The temperature for gate polysilicon 216 deposition is suitably approximately 500 - 800 degrees C, preferably approximately 550 - 650 degrees C, and the resulting thickness of the polysilicon 216 is suitably approximately 500 - 2000 Angstroms. Note that because the previously deposited polysilicon layer 206 is thin (typically < 50 Angstroms), the planarity of the gate poly stack is maintained, which is beneficial for subsequent process steps such as gate poly lithography (not shown). The resulting structure is shown in the cross-sectional view of FIG. 2E. In the resulting structure, the left-hand side 202a of the substrate 202 has thin gate oxide (204) , and the right-hand side 202b of the substrate 202 has thick gate dielectric (212).

The Reference(s), Generally

Jeong 6,780,715 discloses Method for fabricating merged dram with logic semiconductor device. A method is disclosed for fabricating an MDL (Merged DRAM Logic) semiconductor device, in which silicide is formed on a logic region and a memory region selectively for enhancing device reliability. The method includes the steps of (a) providing a substrate having a first region and a second region adjoining the first region, (b) forming a first gate forming material layer in the first region, (c) forming a second gate forming material layer in the first region having the first gate forming material layer formed therein and the second region, (d) selectively patterning the second gate forming material layer to form second gates in the second region and a boundary dummy pattern layer at a boundary area of the first and second regions, and (e) selectively patterning the first gate forming material layer to form first gates in the first region.

Radens 6,388,294 discloses Integrated circuit using damascene gate structure. An integrated circuit device is presented. The integrated circuit device of the present invention comprises a semiconductor substrate having a combination of transistor gates formed using a conventional dielectric-capped gate stack for self-aligned diffusion contacts (SAC) as well as a transistor gate

structure formed by removing the dielectric-cap gate stack from selected regions of the semiconductor substrate and replacing the dielectric-cap gate stack with a second gate conductor which is patterned using a damascene process.

Lin 6,063,670 discloses gate fabrication processes for split-gate transistors. A method for forming an integrated circuit having multiple gate oxide thicknesses is disclosed therein. A circuit (10) is processed up to gate oxide formation. A first gate dielectric (20) is formed. Next, a disposable layer (22) is formed over the first gate dielectric (20). The disposable layer (22) comprises a material that may be removed selectively with respect to silicon and the gate dielectric, such as germanium (Ge). If desired, a second dielectric layer (24) may be formed over the disposable layer (22). A pattern (26) is then formed exposing areas (14) of the circuit where a thinner gate dielectric is desired. The second dielectric layer (24), if it is present, and the disposable layer (22) are removed from the exposed areas. The pattern (26) is then removed. Following pre-gate cleaning, the second gate dielectric (30) is formed. The remaining portions of the disposable layer (22) may be removed either prior to, during, or after the second gate dielectric formation (30). (parentheses with reference numerals in original)

More particularly, in Jeong (columns 7 and 8),

> ... referring to FIG. 4A ...a first gate oxide film 74 with a first thickness and a first gate forming material layer 75 are sequentially formed on the entire surface of the substrate 70. The first gate forming material layer 75 is formed of undoped polysilicon. Then, a first capping layer 76 of oxide, nitride or any other suitable material is formed on the first gate forming material layer 75 for preventing etch damage to the gate layer in the subsequent gate etching process.
>
> Referring to FIG. 4B, a photoresist layer is formed on the entire surface of the resultant structure, and patterned selectively, thereby forming a first photoresist pattern layer 77 only in the logic region 71. Here, the photoresist layer 77 is patterned such that it is absent near the boundary B of the logic region 71. The first capping layer 76, the first gate forming material layer 75, and the first gate oxide film 74 with the first thickness, which

are provided in the memory region 72, are etched selectively by using the first photoresist pattern layer 77 as a mask, so that the substrate 70 in the memory region 72 and the boundary area of the logic region 71 is exposed.

Referring to FIG. 4C, a second gate oxide film 78 with a second thickness thicker than the first thickness of the first gate oxide film 74, a second gate forming material layer 79 for forming a memory, a silicide layer 80 of a refractory metal such as tungsten, and second capping layers 81 and 82 are formed in succession on the entire surface of the substrate 70. In this instance, a polycide structure is employed taking a reliability of the memory and a following capacitor forming process. The second capping layers 81 and 82 are a stack of an oxide film (81) and a nitride film (82), respectively. (emphasis added)

Referring to FIG. 4D, photoresist is applied on the entire surface of the resultant structure and patterned selectively to form a second photoresist pattern layer 83 with a fixed width in a wordline forming region and above the boundary (B) area of the logic region 71 and above the memory region 72 for patterning a wordline in the memory region 72. A stack of the layers 82, 81, 80, 79, and 78 are then etched selectively by using the second photoresist pattern layer 83 as a mask, to form at least one memory gate 84 of a DRAM cell and a boundary dummy pattern layer 85 at the boundary B between the logic and memory regions 71 and 72. In this instance, using the second photoresist pattern layer 83 as a mask, **all the layers 76, 78, 79, 80, 81, and 82 in the non-boundary area of the logic region 71 are removed completely, leaving only the first gate oxide film 74 and the first gate forming material layer 75 therein.** (emphasis added)

Traversing the Rejection(s)

The rejections are primarily based on the Jeong patent. Although some of the initial steps are similar to those of the present invention, the final result is very different. For example comparing Fig 4B from Jeong with FIG. 2A from the present invention shows that at this early intermediate step, both are very similar. However, comparing FIG. 4C/D from Jeong with FIG. 2E from the present invention shows that the final structure that the inventor(s) build using this

method is clearly different from Jeong.

Jeong FIG. 4D shows on the left side, the gate that is formed is the first polysilicon 75 only. The second polysilicon 79 has been completely removed from the left side.
In the present invention, FIG. 2E shows that on the left side, the second polysilicon 216 actually remains as part of the final structure, on top of the thin first polysilicon 206. We specify that 206 is "thin" so that the overall top surface planarity of FIG. 2E is essentially maintained.

In the present application, it is specified that the hard mask 208 is Ge (or could be other material as well). Referring to our Fig 2C, Ge has the beneficial property that the Ge-oxide (214) easily etches / dissolves in water which means we can easily remove 214 (and ultimately 208") easily without harming the dielectric 212. Jeong makes no mention of using Ge as a hard mask - instead they suggest making capping layer 76 oxide or nitride. In either case, it will be nearly impossible to remove the oxidized hardmask or the hardmask itself without etching away 212 dielectric-2 as well.

Generally, in "layman's" terms, in the present invention a first gate oxide 204 is formed in a left-hand portion and a right-hand portion, and then is stripped from the right-hand region, resulting in what you see in FIG. 2A. There is also a first poly layer 206 which remains in the left-hand region. Jeong does this too - see his FIG. 4A - (gate oxide 74, poly 75).

Next, a second dielectric 212 is grown, but this is primarily on the right side, because the hard mask 208 on the left side does not oxidize well. And, jumping ahead, it can be observed that the little bit of oxidation 214 on the left side will be removed (see FIG 2D). Whatever is built up on the left in Jeong is also removed, see his FIG. 4D.

So, what we have both (invention and Jeong) ended up with at this intermediate stage is a thin gate oxide on the left side and a thick gate oxide on the right side.

Then, we (invention) put down a second poly 216 (Fig. 2E) over the whole thing (left and right).

Jeong does this too (79, second poly, see FIG. 4E).

But note in Jeong FIG. 4C, that there is a capping layer 76 (as well as oxide 78) between the first poly 75 and the second poly 79 on the left hand side. This is not a good idea, so Jeong has to strip everything over the first poly 75 on the left hand side - see his FIG. 4D.

In the present invention, the hard mask 208 (208", 214) is removed between 2C and 2D, prior to applying the second poly 216 in 2E, and we end up with second poly 216 on first poly 206 on the left hand side. Jeong can't do this.

The claims are amended accordingly.

In claim 1, the limitation of "after removing the hard mask depositing a second layer of polysilicon in both the first and second areas of the substrate" has been added. For the reasons set forth above, none of the references taken alone or in combination meet this limitation and therefore claim 1 should be deemed allowable.

Claims 3-14 are dependent upon claim 1 and should also be deemed allowable.
Independent Claim 15 has been amended to set forth the method of forming gate dielectrics on a semiconductor substrate. The method includes the steps of forming a first gate dielectric on the top surface of the substrate; depositing a first layer of polysilicon over the first gate dielectric; protecting the first gate dielectric by forming a sacrificial hard mask over a selected area of the first layer of polysilicon; forming a second gate dielectric in the second area; removing the sacrificial hard mask; and depositing a second layer of polysilicon over the second gate dielectric and over the first layer of polysilicon. For the reasons set forth above, none of the references taken alone or in combination meet these limitations and therefore claim 15 should be deemed allowable.

Claims 21- 26 are dependent upon claim 15 and should therefore also be allowable.
Newly-presented Claim 22 depends upon claim 15 and includes the first gate dielectric being a

material selected from the group consisting of silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material. Since claim 21 depends upon claim 15, it should also be allowable.

Newly-presented Claim 22 depends upon claim 15 and includes the second gate dielectric being a material selected from the group consisting of silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material. Since claim 22 depends upon claim 15, it should also be allowable.

Newly-presented Claim 23 depends upon claim 15 and includes the sacrificial hard mask being a material selected from the group consisting of germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO2, Si3N4, and other materials that are easy to remove from a silicon wafer without leaving a residue. Since claim 23 depends upon claim 15, it should also be allowable.

Newly-presented Claim 24 depends upon claim 15 and includes the second gate dielectric being formed by a process selected from the group consisting of: rapid thermal oxidation (RTO) in NO, N2O, NH3, O2 (500-1100 degrees C); plasma nitridation treatment on base oxide (25 - 800 degrees C); and plasma oxidation; UV oxidation; and atomic layer deposition. Since claim 24 depends upon claim 15, it should also be allowable.

Newly-presented Claim 25 depends upon claim 15 and includes the first gate dielectric being thinner than the second gate dielectric. Since claim 25 depends upon claim 15, it should also be allowable.

Newly-presented Claim 26 depends upon claim 15 and includes the first gate dielectric being a high-k material. Since claim 26 depends upon claim 15, it should also be allowable.

Claims 2, 16-20 (six total) are canceled and claims 21-26 (six total) are presented.

In light of the comments traversing Jeong, the remaining references need not be discussed in any great detail.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Howard M. Cohn
Registration No. 25,808

Howard M. Cohn
21625 Chagrin Blvd. Suite 220
Cleveland, OH 44122
Voice (216) 752-0955
Fax (216) 752-0957

CERTIFICATE OF TRANSMISSION BY FACSIMILE

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (Fax No. 571-273-8300) on April 26, 2006.

Name of Person Signing Certificate : Howard M. Cohn

Signature :

Date of Person signing : 26 April 2006

C:\Documents and Settings\Server\My Documents\IBM\IBM-104\ibm104 2am 042506.doc